Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical/typographical errors.

The claims have been amended and new claims added to more clearly claim Applicants invention. Support for the amended and newly drafted claims are found in the original claims and/or specification. Specifically, support for claims 1, 25 and new claims e.g., 23, 24, 30 and 31 are found in paragraphs 0033, 0034, and 0035 beginning on page 17:

"In the method according to the present invention, a first photoresist layer 20 (bottom image layer) of a **non-silicon containing organic material**, for example a **resinous I-line photoresist or acrylic polymer** is deposited over **the ILD layer** 18 by a typical spin coating method. The photoresist layer 20 need not be photoactive, for example, need not contain a photo-generated acid. **One exemplary organic resin** for photoresist layer 20 may further include a **polyvinyl alcohol resin**. Photoresist layer 20 is preferably deposited to a thickness of between about 1000 Angstroms and 5000 Angstroms. The photoresist layer 20 is preferably baked at a temperature of between about 120 °C and 130 °C for a duration of between about 2 and 3 minutes.

A second photoresist layer 22 (top image layer) with a thickness of about 500 Angstroms to about 3000 Angstroms, preferably thinner than bottom image layer 20, is then formed over bottom image layer 20 by a similar method. The top image layer 22 is preferably a DUV photoresist **formed of silicon containing organic including silicon monomers being photoactive at, for example, 193 nm and 157 nm.** Exemplary photoresists include, for example, a terpolymer photoresist of methacrylic acid. Top image photoresist layer 22 is preferably applied by spin coating and baked at a temperature of between about 120 °C and 130 °C for a duration of between about 2 and 3 minutes.

Less preferably, **a non-silicon containing photoresist may be used for top image layer 22 and subjected to a silylation process to form a silicon containing photoresist.**"

The remaining amendments and newly drafted claims find support in the original claims and/or the specification. No new matter has been entered.

Claim Rejections under 35 USC 112

Claim 4 has been cancelled thereby overcoming Examiners rejection.

Claim Rejections under 35 USC 102(e)

Claims 1-5, 7-10, 13-15, and 17 through 20 stand rejected under 35 USC 102(e) as being anticipated by Shibata (U.S. Pub. No. 2002/00036183) published March 28, 2002.

Shibata discloses a method for forming a reverse pattern in a lower resist layer compared to the pattern in the upper resist layer (see e.g., Fig 2 series, Fig 3 series and Fig 4 series). Shibata discloses a prior art method (Fig 1 series, e.g., paragraph 005) whereby a multi-resist patterning method including an SOG film sandwiched between a lower resist layer and an upper resist layer (see e.g., Fig 1C, and paragraph 005). Shibata teaches away from this method by pointing out that the SOG film fluctuates in dimension (paragraphs 0010, 0012) and undesirably affects dimensions in the upper resist layer. Shibata also points teaches away from a two layer resist method since sufficient etching resistance is generally not provided for the upper resist layer leading to deterioration of the upper resist layer.

In the method of Shibata an upper resist layer overlying a lower resist layer is patterned followed by depositing a Si, Al, or Ti containing polymer covering layer (disclosed to be polysesquioxane) which fills the patterned openings (see e.g., paragraphs 0034 -0045) followed by removing the covering layer above the patterned opening level (planarizing) by a CMP or wet etching method (paragraphs 0043, 0045, 0046). Significantly, the covering layer (polysesquioxane) is not a photoresist. A portion of the 'silicon-containing' covering layer is left within the

patterned portions of the upper resist layer and is then used as a mask for RIE etching the unpatterned portions of the upper and lower resist layers to form a reversed pattern etching mask (see e.g., paragraph 0101). Shibata alternatively teaches that a fluorine containing etchback process may be used to **etchback** the covering layer(see e.g., paragraph 0100) but that the wet etching process for etching the silicon containing covering layer is simpler and more efficient than an RIE process (see paragraph 0068). Shibata also discloses an RIE etching process consisting of a mixture of O_2/N_2 to etch through unpatterned portions of resist layers 1 and 2 using the silicon containing covering layer as a reverse mask (see e.g., paragraph 0116).

Shibata does not disclose a bi-layer resist patterning process, or disclose a silicon containing upper **resist** layer that is patterned according to a photolithographic and wet development process, or where an N_2/O_2 etching chemistry is then used to etch through the underlying resist layer according to the overlying pattern, as claimed by Applicants in their disclosed and claimed invention.

The teachings of Shibata are clearly insufficient to make out a case of anticipation under 35 USC 102(e).

The teachings of Shibata further do not teach or discuss the limitations in the relevant dependent claims as claimed by Applicants.

Rather Shibata specifically teaches away from using a bi-layer resist by teaching that a bi-layer resist method has the problems of deteriorating the upper resist layer due to insufficient etching resistance in a dry development process. Neither the prior art disclosed in Shibata nor the teachings of Shibata recognize or solve the problem that Applicants have recognized and solved by their disclosed and claimed invention:

"A method for semiconductor device feature development using a bi-layer photoresist to improve an etching resolution and reduce particulate contamination"

Claim Rejections under 35 USC 103(a)

Claims 2 and 4, stand rejected under 35 USC 103(a) as being unpatentable over Shibata, above, and further in view of Smith (U.S. Pat No. 6,388,226).

The comments made above with respect to Shibata are reiterated.

Smith discloses an improved low-field toroidal plasma source (see Abstract). Smith discloses that the plasma source can be operated to increase the etch rate of organic materials (see Abstract). Smith generally discloses that oxygen is useful for removing photoresist in an etching process (col 1, lines 60-65) and generally discloses that adding a noble gas such as argon to a plasma can increase the output of active species (col 15, lines 29-43) for example in a nitrogen/oxygen plasma. Smith does not teach using a nitrogen/oxygen plasma to etch photoresist or disclose a bi-layer or multi-layer resist or a method for developing or etching the resist. There is no motivation to combine Smith with Shibata, and in any event, does not produce Applicants disclosed and claimed invention. To establish a *prima facie* case of obviousness effective variable argument requires a proper motivation to combine teachings followed by producing Applicants claimed invention by such combination, neither of which is present in the instant combination.

"We do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

Claims 8-13, 18, and 20 stand rejected under 35 USC 103(a) as being unpatentable over Shibata in view of Smith, above, and further in view of Fujimura (US 4,938, 839)

Fujimura discloses a method whereby during an oxygen ashing process of a resist layer, a wafer support is cooled to prevent the photoresist from overheating and sticking to the wafer (see Abstract). Fujimura does not teach using a nitrogen/oxygen plasma to etch photoresist or disclose a bi-layer or multi-layer resist, a silicon containing photoresist or a method for developing or etching the resist. Fujimura does not teach or suggest an in-situ ashing process for removing photoresist while simultaneously cleaning contact surfaces. Shibata does not teach or disclose an ashing process or a plasma cleaning process. There is no motivation to combine Fujimara with Shibata or Smith, and in any event, does not produce Applicants disclosed and claimed invention.

Examiner contends with respect to claim 20 where Applicants claim that the various process steps are carried out in-situ in a continuous process, that "it is known is the art that this will decrease the processing time required for the semiconductor devices being manufactured." Applicants do not concede the accuracy of this statement nor does Examiner cite any reference

or support for this statement. In fact, Shibata teaches away from such a conclusion by teaching that a wet etching or CMP process for removing the silicon containing (not a photoresist) covering layer is preferred to an RIE etchback process (using fluorocarbons) "to save manufacturing cost and improve throughput and productivity" (see paragraph 0068). Further the alternative RIE etchback process using fluorocarbons to etchback the silicon containing layer (not a photoresist) taught by Shibata teaches away from Applicants in-situ oxygen ashing process to remove the upper silicon containing photoresist and lower organic resinous layer (e.g., photoresist).

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.** *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

With respect to the remaining independent claims, Applicants generally reiterate the above arguments and reiterate that there is no motivation for combining the teachings of the references cited, and further, that such combination does not produce Applicants invention.

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

With respect to the remaining independent claims, since neither Shibata nor any combination of the recited references produce Applicants claimed invention, thereby failing to make out a *prima facie* case of obviousness, neither has a *prima facie* case of obviousness been made out with respect to the amended and newly drafted dependent claims.

The Claims have been amended to clarify Applicants claimed invention and newly drafted claims added. A favorable consideration of Applicants' claims is respectfully requested. The Commissioner is hereby authorized to charge Deposit Account No. 50-0484 any fee as a result of this amendment.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his

Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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